Commodity Specification

C.S. No.	Rev.	Date
RCS-MM-12485	0	Apr. 24, 2009

Apple Inc.

Type
R5H30201NA04NQ09
(Pb-Free T.)

※【RoHS compliant】Pb-FreeT. means product keeps terminals treated by Lead Free materials.

Signed

NOTICE
Please check this C.S. and return this copy with your signature to acknowlege your approval.

Starting from April 1, 2003, Renesas Technology Corp. takes over the responsibility for attached drawings from Hitachi, Ltd., due to the corporate division.

RENESAS

Renesas Technology Corp.

MCU Business Group

Tatsumi Sueyoshi

C.S.	History

Rev.	Date	Item	Record of revision
0	2009.04.24	Crea.	

Cautions

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Remarks

Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{in}	−0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	−25 to +85	°C
Storage temperature	T_{stg}	−55 to +85	°C

Note: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the recommended operating conditions. Exceeding these conditions could affect the reliability of the chip.

DC Characteristics

Table 1 DC Characteristics

Conditions: V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, T_a = –25 to +85°C, unless otherwise specified.

Item			Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input high voltage	$\overline{RES}$		V_{IH}	V_{CC} = 1.8 to 2.2 V	V_{CC} × 0.85	—	V_{CC} + 0.3	V
	P1, P2, P3, P4			V_{CC} = 2.2 to 3.6 V	V_{CC} × 0.7	—	V_{CC} + 0.3	
Input low voltage	$\overline{RES}$		V_{IL}	V_{CC} = 1.8 to 2.2 V	–0.3	—	0.2	V
	P1, P2, P3, P4			V_{CC} = 2.2 to 3.6 V	–0.3	—	V_{CC} × 0.2	
Output high voltage	P1, P2, P3, P4		V_{OH}	I_{OH} = –200 µA	V_{CC} × 0.7	—	V_{CC}	V
Output low voltage	I/O ports		V_{OL}	I_{OL} = 1 mA	0	—	0.4	V
Input leakage current	P1, P2, P3, P4		$\|I_{in}\|$	V_{in} = 0.5 to V_{CC} – 0.5 V	—	—	10	µA
Input pull-up MOS current*1	$\overline{RES}$		$-I_p$	V_{in} = 0 V	—	—	150	µA
	P1, P2, P3, P4				—	—	150	
Supply Current*2	CPU half of the external clock/ external clock	Coprocessor stops*3	I_{CC}		—	—	7.5	mA
	CPU multiplied by one with PLL	Exclusive mode*3			—	—	7.5	
	CPU multiplied by two with PLL	Normal speed of coprocessor in maximum mode*3			—	—	7.5	
Supply Current*2	Sleep mode 1		I_{CC}	V_{in} (I/O ports and $\overline{RES}$) = V_{CC} - 0.5 V to V_{CC} or I/O ports open*1 $T_a \leq 50°C$	—	—	100	µA
				V_{in} (I/O ports and $\overline{RES}$) = V_{CC} - 0.5 V to V_{CC} or I/O ports open*1 $T_a \geq 50°C$	—	—	200	
Pin capacitance			Cp	V_{in} = 0 V, f_{CLK} = 1 MHz, T_a = 25°C	—	—	15	pF

Notes: 1. The input pull-up MOS's in the $\overline{RES}$ is always turned on, even in sleep mode 1 and sleep mode 2. To avoid the input pull-up MOS current, the $\overline{RES}$ must be kept high during sleep mode 1 and sleep mode 2.

2. V_{IHmin} = V_{CC} – 0.5 V, V_{ILmax} = 0.5 V, and values are when all output pins are unloaded.
3. These are operating modes other than sleep mode 1.

AC Characteristics

Table 1 AC Characteristics

Conditions: V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, T_a = –25 to +85°C, unless otherwise specified.

Item		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Clock cycle time (CPUCS = 0)		t_{cyc}		278	333	417	ns
Clock cycle time (CPUCS = 1)				139	166	208	
Clock rise time		t_{Cr}	Figure 1	—	—	1.0	µs
I/O port input fall time		t_f	Figure 1	—	—	1.0	µs
$\overline{RES}$ pulse width	Cold reset	t_{RWL1}	Figure 2	500	—	—	µs
	Warm reset	t_{RWL2}	Figure 2	400	—	—	t_{cyc}
EEPROM write time	Normal rewriting mode	t_{EPW}	Rewrite	—	—	3	ms
			Erase	—	—	1.5	ms
Interrupt pulse width ($\overline{IRQ}$)	Sleep mode 2	t_{IRQW}	Figure 3	4	—	—	t_{cyc}
	Other modes			400	—	—	ns

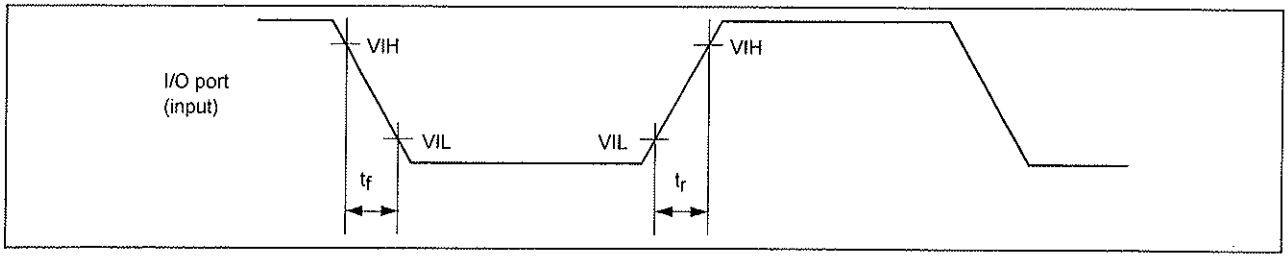


Figure.1 I/O Port Input Waveform

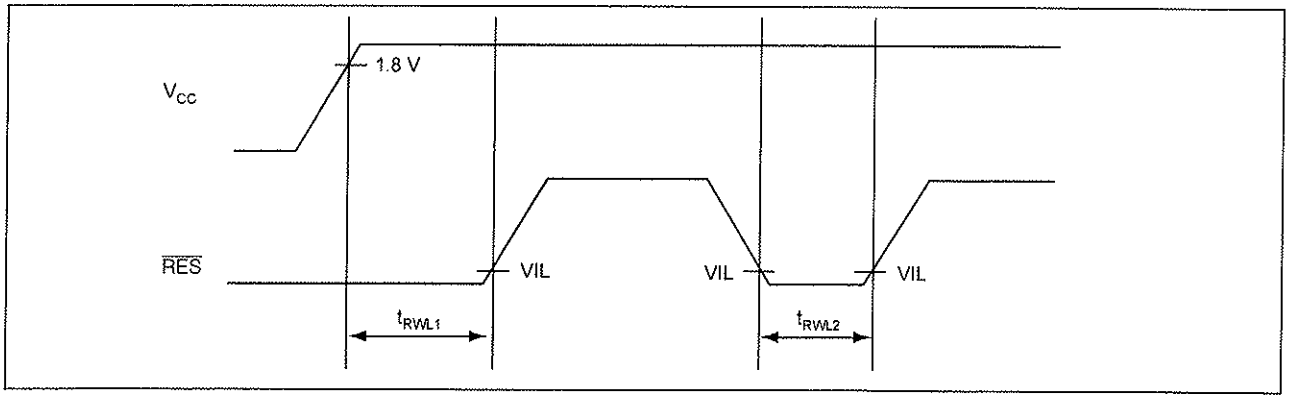


Figure.2 Power ON/OFF and RES Input Timing

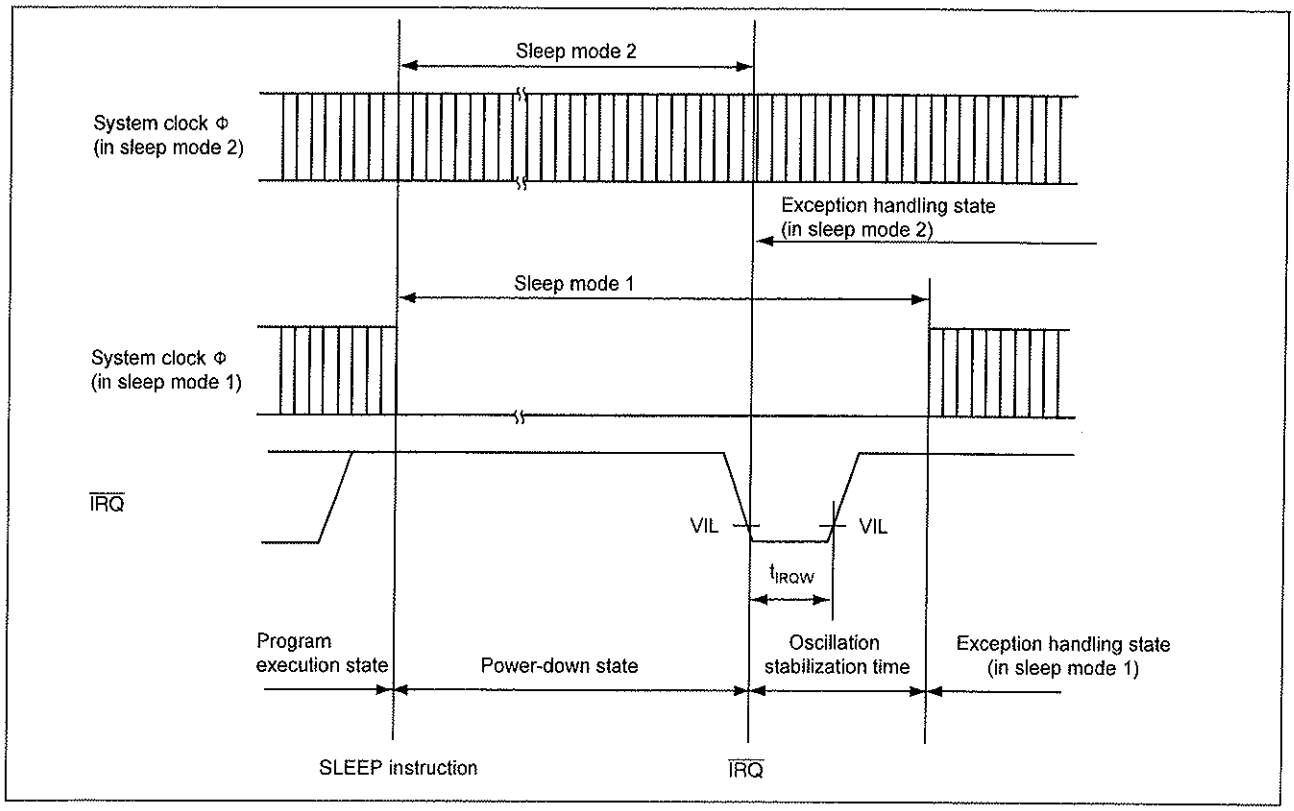


Figure 3 Interrupt Timing in Sleep Mode 1 and Sleep Mode 2

Reset Circuit Characteristics

Table 1 Reset Circuit Characteristics

Conditions: V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, T_a = –25 to +85°C, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power-on reset effective voltage	V_{POR1}	Figure 1	—	—	0.1	V
Power-on reset release voltage rise time	t_{PWON1}	Figure 1 $t_{POR1} \geq$ 1s*	—	—	0.5	ms
Power-on reset release voltage rise time	t_{PWON1}	Figure 1 $t_{POR1} \geq$ 10s*	—	—	1	ms
Power-on reset release time	t_{PRST}	Figure 1	—	—	500	µs

Note: t_{POR1} is the time needed to enable the power-on reset by keeping the external power supply Vcc to lower than the effective voltage (V_{POR1}).

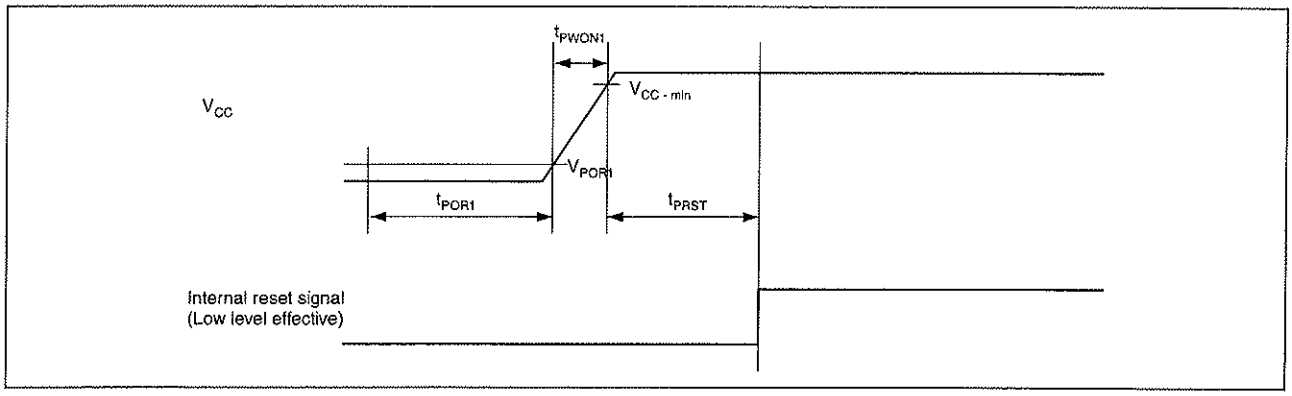


Figure 1 Power-On Reset Timing

Voltage Monitoring Circuit

Table 1 Voltage Monitoring Circuit Characteristics

Conditions: V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, T_a = –25 to +85°C, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Voltage detect level	V_{DET0}	Figure 1	1.9	2.3	2.6	V

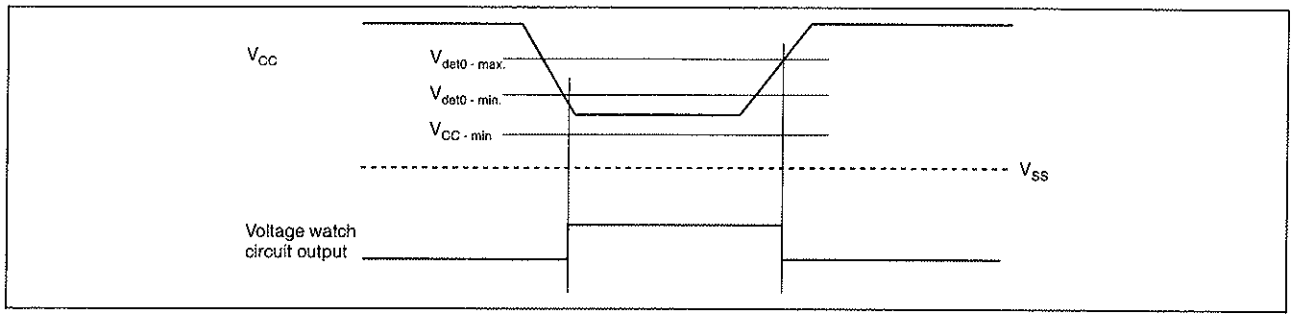


Figure 1 Voltage Monitoring Circuit Timing

Erase/Write cycle endurance and Data retention time of EEPROM are specified as follows.

Item	Condition		Rating
Erase/Write cycle endurance of EEPROM *1	Page rewrite *2	-25℃ to +85℃	1×10^5 times
Data retention time			10 years

Note; *1 It is assumed the failure rate is 1% or below in case of reliability standard 90%.

*2 One page rewriting is counted as one time.

Block Diagram

Figure 1 is a block diagram of this LSI.

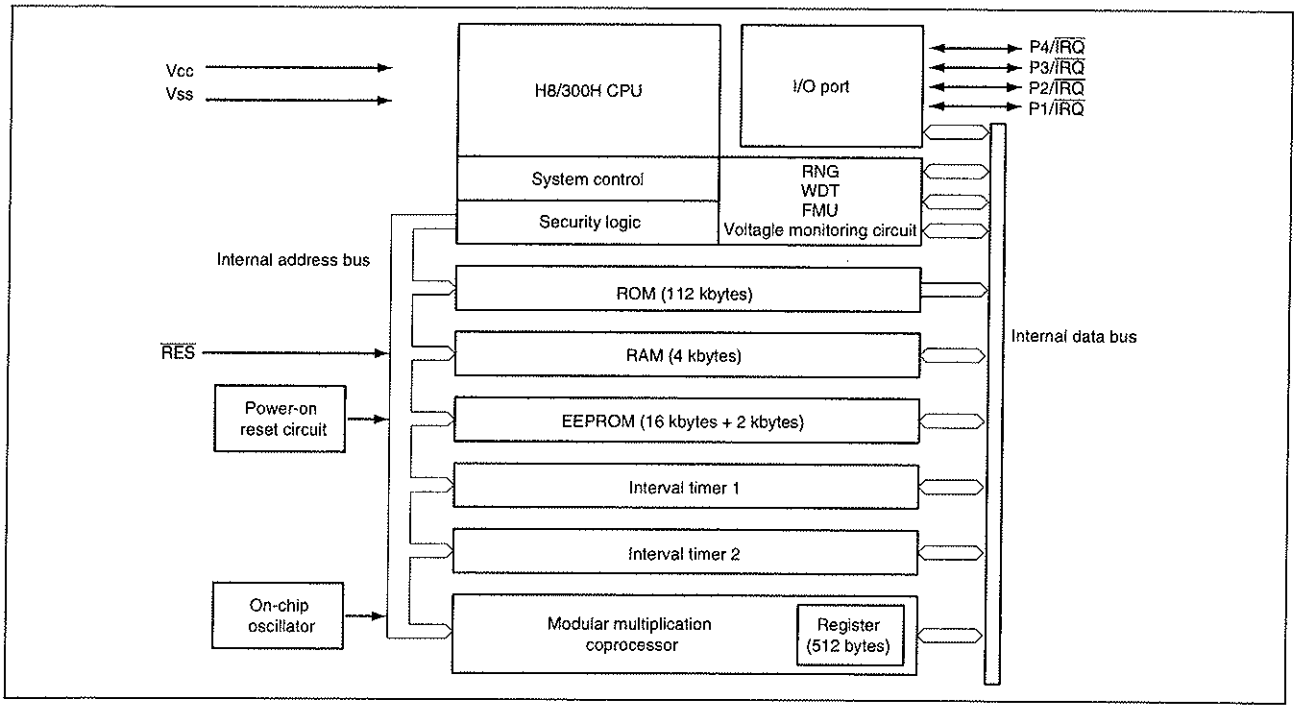


Figure 1 Block Diagram

Pin Assignment

Figure 1 shows the pin arrangement of this LSI.

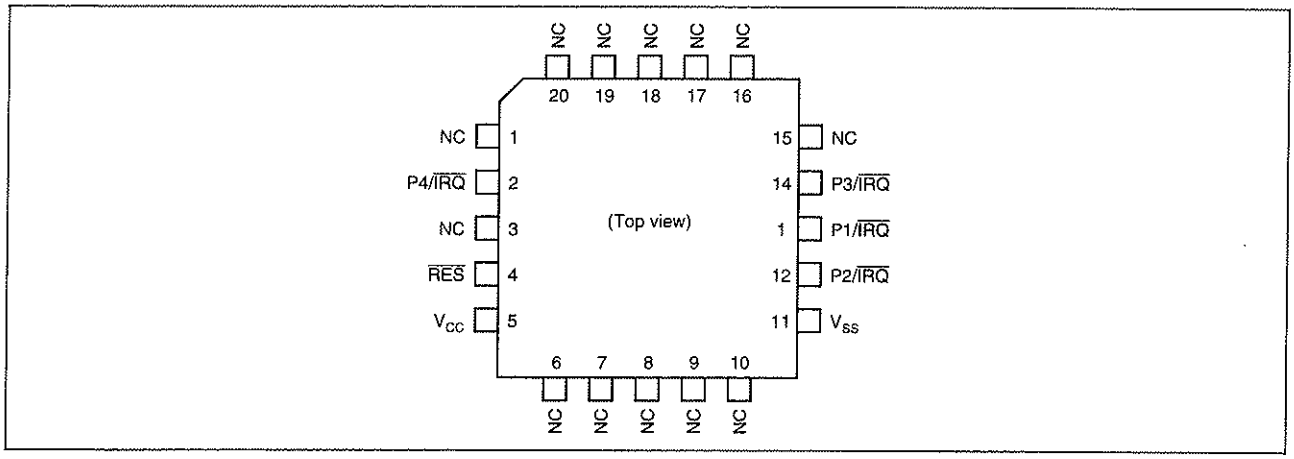
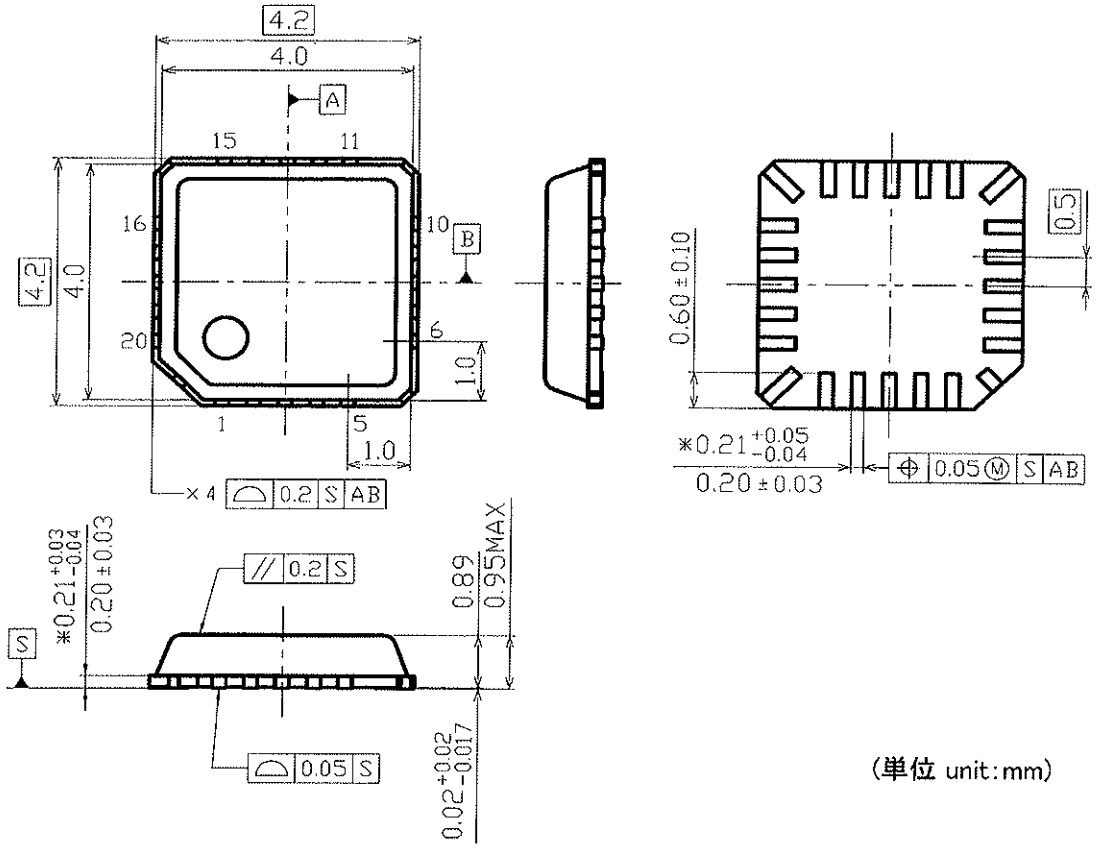


Figure 1 Pin Assignment (TNP-20CV)

APPD. CHKD. REVD. DATE REVISIONS SYM. NPL

Package Dimensions



(単位 unit:mm)

パッケージコード (Package CODE)	PVQN0020KD-A
JEITAコード (JEITA CODE)	—
JEDECコード (JEDEC CODE)	—
質量 (Mass)	0.04 g

＊めっき厚含み寸法
素材寸法

＊ Dimension including the plating thickness
Base material dimension

MM5 1
MQ 1
PROVI. SECT. co py

REMARKS

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-OUTLN

顧客向け外形寸法図

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	50	AN	528	E	PKGFTR 1228

Renesas Technology Corp.

343 4Q02211

SH. 1 / E

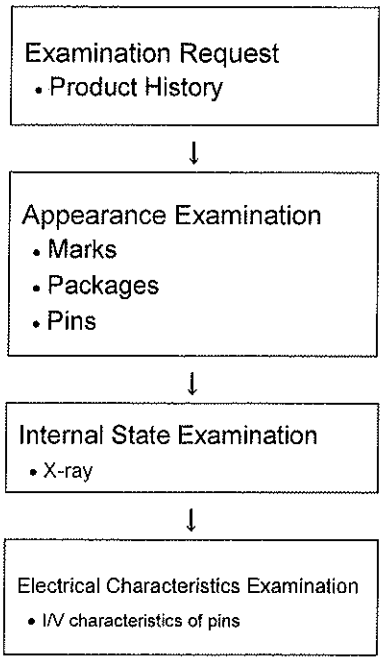
D.CHKD

D C B A PVQN0020KD-A Gr. PKG CODE

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

Returns Analysis

This product has an advanced security function against unauthorized attacks. Therefore, unlike common MCU products, it is impossible to carry out a functional test with an LSI tester against shipped products.
Returns analysis flow chart of this product is illustrated below.



Returns Analysis Flow Chart
(Examination and Evaluation Method)

1

リフロー法推奨条件　(小型パッケージ)
Recommended Reflow Soldering Conditions

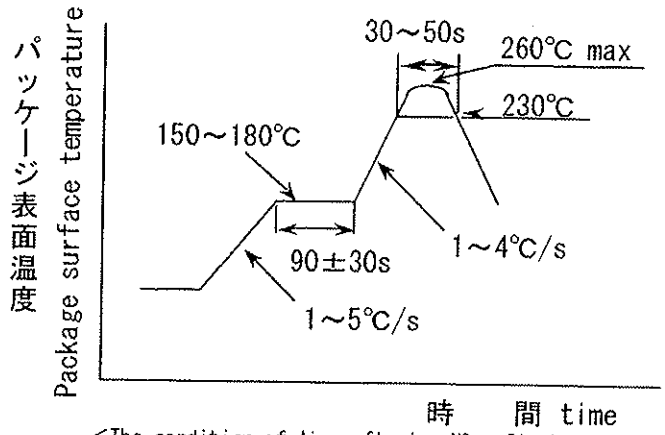
防湿包装開封後は再吸湿を避けるため、防湿包装開封後の保管条件以内にリフロー実装して下さい。
またそれ以上経過した場合はベーク条件の示すベークを行って下さい。

After opening the moisture proof packing, parts must be installed at the condition , the keeping condition after opening dry packing, against re- moisturized.
If the device has been stored longer than the specified time after opening packing, parts must be baked at the condition of the baking condition.

(1) 部品耐熱性　　Parts capacity of heat proof

エアリフロー、N2リフロー　:パッケージ表面温度 =260℃ max,
230℃以上の時間 =30～50秒

Air reflowing ,N2 reflowing　:Package surface temperature =260℃ max,
Over 230℃ time=30～50s



<The condition of Air reflowing, N2 reflowing>
<小型パッケージのエアリフロー、N2リフロー推奨条件>

(2) リフロー回数　:　3回　　(防湿包装開封後の保管条件以内)

Reflowing times :　3times　　(While the keeping condition after opening dry packing)

REVISIONS
P.1, W#PKGFTR, S#4179

MHSわ	わ
MHSM	1
Mタカサキ	D
Mチョウ L	D
MW	D
MM3	1
MM2	1
MM1	1
MA	1
MQ	1
PROVI. SECT.	co py

REMARKS　Pb－Free

DWN.　CHKD.　APPD.　REGD.　PROJECTION　SCALE NTS

TITLE
FTR-REFL-COND
顧客向けリフロー条件

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	5Z	B2	528	E	PKGFTR 4179

Renesas Technology Corp.

343　4Q01178

SH. 1 / E

D.CHKD　D C B A GENERAL Gr. 区分(GROUP)

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

△2

防湿包装開封前の保管について
Storage Before the Dry Pack is Opened

防湿包装開封前の保管期限は5～35℃、85%RH以下で2年です。
The time limit to leave the packages in a dry pack is 2 years, provided that the temperature is between 5 to 35℃ and the relative humidity is 85% or less.

APPD.	CHKD.	REVD.	DATE	REVISIONS	NPL	SYM
				P.1 . W#PKGFTR, S#4782	1	△2

MHSD	D
Mﾁｮｳﾚ	D
MW	D
MQ	1
MM3	1
MM2	1
MM1	1
MHSM	1
MA	1
PROVI. SECT.	copy

D.CHKD

D	C	B	A GENERAL	Gr. 区分(GROUP)

REMARKS: 防湿包装開封前

DWN. / CHKD. / APPD.

PROJECTION

SCALE NTS

REGD.

TITLE: FTR-STRG-COND
顧客向け保管条件

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	50	AN	528	E	PKGFTR 4782

Renesas Technology Corp.

343 4Q00876

SH. 1 / E

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

1

防湿包装開封後の保管及び取り扱いについて
Storage and Handling After the Moisture-proof Bag is Opened

防湿包装開封後は吸湿を避けるため、下記条件にて保管してください。
Parts must be kept as below after opening dry packing against re-moisturized.

項目	条件	備　考
温度 Temperature	5℃～30℃	
湿度 Humidity	60%RH以下 60% RH or less	
時間＊ Time	168時間以内 168 hours or less	＊開封後～最終リフローはんだ付け完了までの時間 This refers to the total time between opening the moisture-proof bag and completing the final reflow soldering process.

REVISIONS
P.1 , W#PKGFTR, S#4180

SYM. N'PL 1 1

MHSD	D
MチョウL	D
MW	D
MQ	1
MM3	1
MM2	1
MM1	1
MHSM	1
MA	1
PROVI. SECT.	∞ PV

REMARKS 防湿包装開封後

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE
FTR-STRG-COND
顧客向け保管条件

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	50	AN	528	E	PKGFTR 4180

Renesas Technology Corp.

343 4Q00877

SH. 1 / E

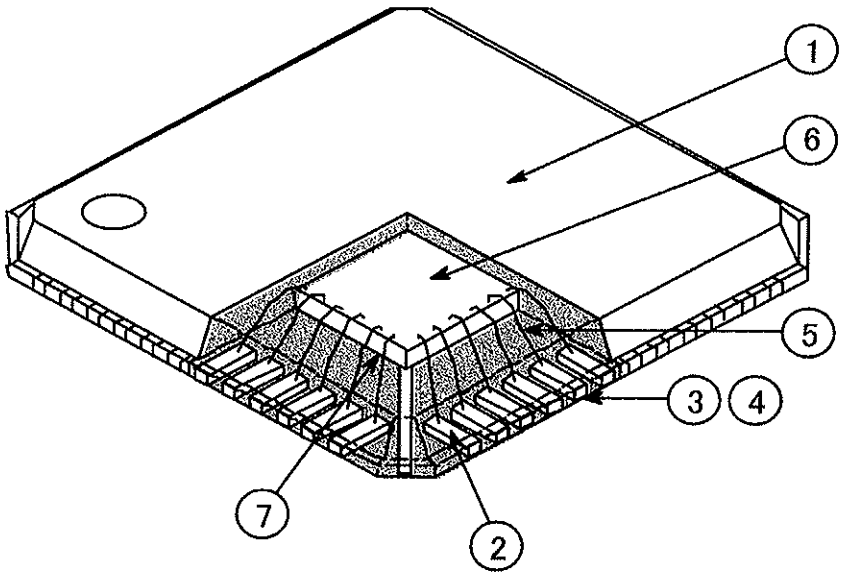
D.CHKD

D	C	B	A	Gr.
			GENERAL	区分(GROUP)

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE REVISIONS SYM. N.PL

QFN内部構造図 (QFN Internal structure)



番号 (No.)	部分 (Part)	材質 (Material)
①	封止樹脂 (Molding compound)	エポキシ樹脂 (Epoxy) 難燃性レベル (UL-level) UL-94V0
②	インナーリード処理 (Inner lead finish)	ニッケル/パラジウム/金 めっき (Ni/Pd/Au plating)
③	アウターリード処理 (Outer lead finish)	ニッケル/パラジウム/金 めっき (Ni/Pd/Au plating)
④	リード (Lead)	銅合金 (Copper Alloy)
⑤	ボンディングワイヤ (Bonding wire)	金 (Gold)
⑥	チップ (Die)	シリコン (Silicon)
⑦	ダイボンディング材 (Die bonding)	樹脂ペースト (Organic adhesive)

MM5 1
MQ 1
PROVI. SECT. copy

REMARKS

DWN. CHKD. APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-STRCT

QFN内部構造図

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	03	AN	528	E	PKGFTR 1228

Renesas Technology Corp.

343 4Q02214

SH. 1 E

D.CHKD D C B A QFN Gr. PKG

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

APPD. CHKD. REVD. DATE

REVISIONS

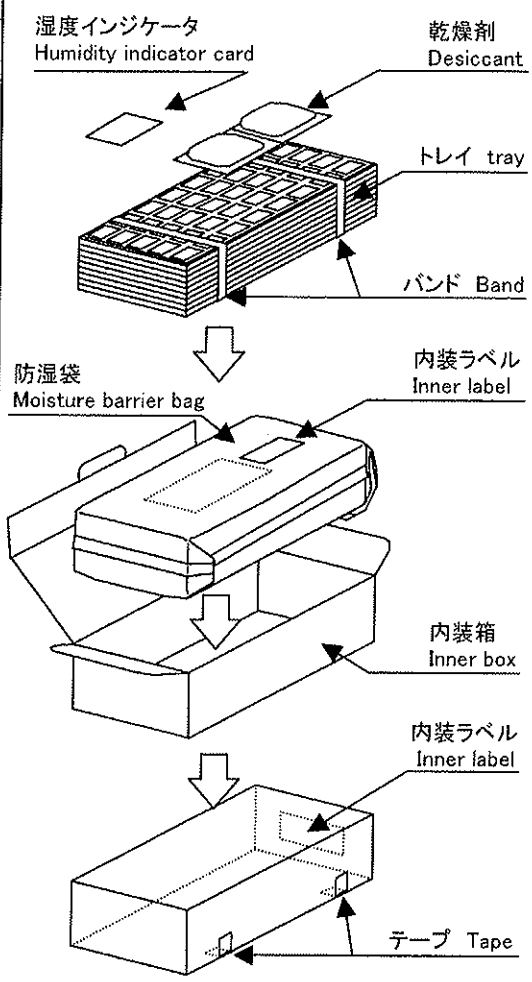
P.1 , W#PKGFTR, S#4623

SYM. N PL 1 / 5

5

トレイ包装仕様 Tray packing specification

(a)包装フロー Packing flow



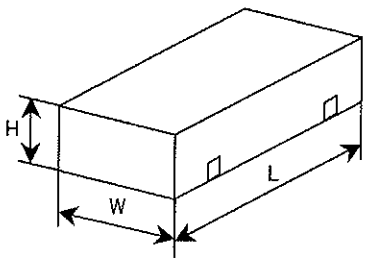
(b)内装ラベル印字内容例

Example of Inner label content of print

略号 Abbreviation	データ名 Date name	備考 note
P/N	顧客型名 Customer No.	必要な場合に表示 Display when it is necessary
PID	-	弊社管理コード For our management
D/N	製造者型名 Manufacture No.	-
QTY	数量 Quantity	-
SPN	-	弊社管理コード For our management
WP	前工程生産国(若しくは地域) Wafer Process conutry (or region) name	必要な場合に限り表示 Display only when it is necessary
AS	後工程生産国(若しくは地域) Assembled conutry (or region) name	必要な場合に表示 Display when it is necessary
(PARTIAL)	端数表示 Partial display	必要な場合に表示 Display when it is necessary
T/C	トレースコード Trace Code	-
S.LOT	-	弊社管理コード For our management
Pb-Free T.	鉛フリー表示 Pb-Free display	製品が無鉛端子の場合に表示 Display when product is Pb-free terminal
MS Level	開封後条件 Condition after opening	必要な場合に表示 Display when it is necessary

一内装が複数ロットで構成される場合、ロットや数量情報をラベル上部に記載する場合があります。
When one interior is composed of two or more lots, information of lots or quantities might be described in the upper part of the label.

(c)内装箱サイズ Inner box size



unit : mm

L	W	H
330	152	75

箱の寸法は参考値です。
現物の寸法とは異なる場合がありますのでご了承願います。
The size of a box is a reference value and may differ from an actual size.

MチョウL D
MQ 1
PROVI. SECT. co py

REMARKS

DWN.
CHKD.
APPD.

PROJECTION

SCALE NTS

REGD.

TITLE

FTR-PCKNG

顧客向け包装図

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	50	61	- - -, 3K00	E	PKGFTR 4623

Renesas Technology Corp.

343 4Q01448

SH. 1 / E

D.CHKD

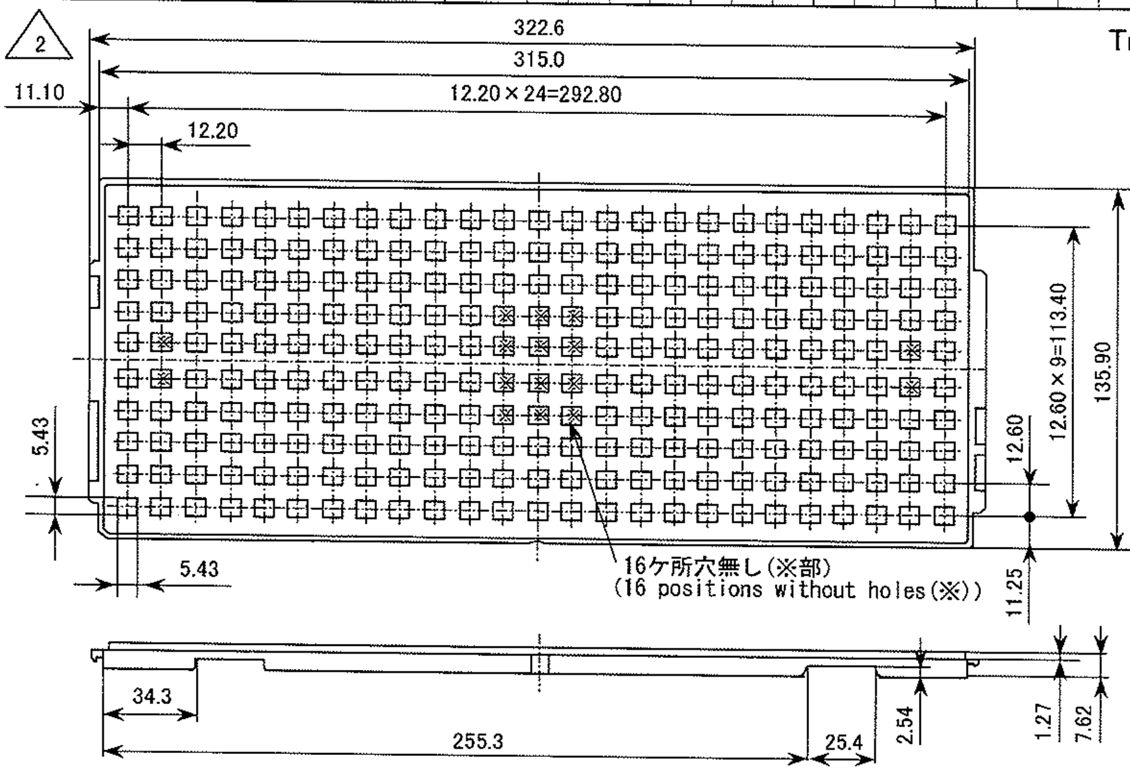
D	C	B	A	Gr.
			TRAY-DRY-RT01	TYPE

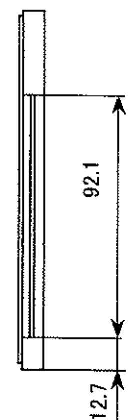
1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

DWN.:Y.Suzuki CHKD.:K.Akiyama APPD.:K.Goto REGD.2009.02.16

D.CHKD.			PROVI. SECT.	MQ	Mチョウし
			Co PY	1	D

SYM.	N.PL	REVISIONS	DATE	REVD.	CHKD.	APPD.
2	2	P.1 , W#PKGFTR, S#4966				





Tray Specifications

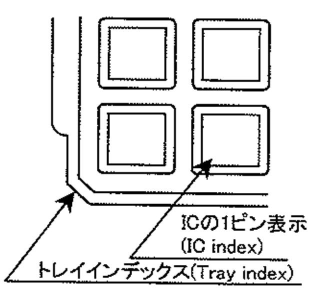
型名 (Tray type)	FT73
材質 (Material)	カーボンPPE (carbon PPE)
耐熱性 (Heat proof)	150°C MAX, 4h (130°C MAX, 24h)
表面抵抗 (Surface resistance value)	$1\times10^9\Omega$／□未満 (Less than $1\times10^9\Omega$／□)
パッケージコード (Package code)	PVQN0020KB-A (TNP-20C,TNP-20CV) PUQN0020KA-A PVQN0020KD-A
最大収納数 (Maximum storage No)	250 IC/トレイ 2000 IC/内装箱 (250 IC/Tray 2000 IC/inside box)

2

単位:mm (Unit)

※寸法値は設計値であり、保証値ではありません。
This tray size is plan and not gurantee.

ICのトレイ収納方向(IC placement direction)



トレイのインデックス(図中の左下)に対して ICの1ピンが 同じ方向(左下)に なる様配列しています。

IC's are placed such that IC 1st pin the same direction to tray index (bottom left).

Gr.	TYPE
A	FT73
B	
C	
D	
E	

REMARKS

DWN.	
CHKD.	
APPD.	

PROJECTION

SCALE NTS

REGD.

TITLE
FTR-TRAY-OUTLN
顧客向けトレイ外形図

DWG.STAMP

SD	TYPE	D.D	CLASS.	MD	WORK-SPEC No.
E	03	6G		E	PKGFTR 4966

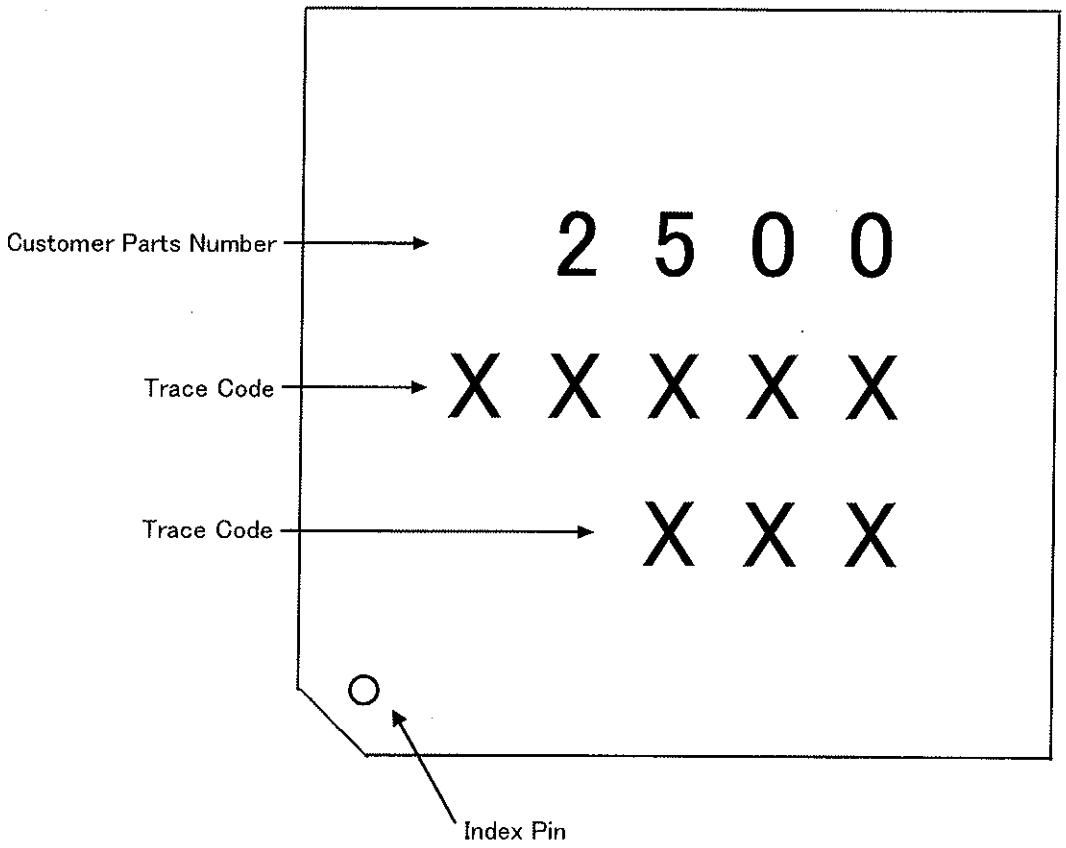
343 4Q01651

SH. 1 E

Renesas Technology Corp.

1234567890 ABCDEFGHIJKLMNOPQRSTUVWXYZ

C.S	Marking Example



To:AVNET

Preliminary

Date: 2008/1/31

Investigation by Renesas standard format on constituents of products(Reply)

Please find below information on all constituents of our semiconductor product R5H30201NA04NQXX (Renesas part no.). If you require this information to be provided in the format designated by you, please inform our sales department of your request. In this case, we ask that you give us an extra time to meet your requirements.
We confirm that the materials stipulated in Montreal Protocol (Level 1) have not been used in the production of R5H30201NA04NQXX (Renesas part no.).
We also confirm that the product does not include any of the materials stipulated in EU RoHS Directives.

CH07-2132

PART	SUBSTANCE	CAS_NO	RENE_CODE	MASS_MG	RATIO	RATIO_P	PURPOSE
chip	Silicon	7440-21-3	C020001	4.064948	11.6000	99.4000	wafers
chip	Arsenic	7440-38-2	C030001	0.000020	0.0001	0.0005	dopant
chip	Boron	7440-42-8	C040001	0.000409	0.0012	0.0100	dopant et.al.
chip	Phosphorus	7723-14-0	C050003	0.001023	0.0029	0.0250	dopant et.al.
chip	Copper	7440-50-8	C160001	0.000123	0.0004	0.0030	wiring material
chip	Aluminum	7429-90-5	C210001	0.024546	0.0701	0.6000	wiring material
			sub_total	4.091070	11.7000	100.0000	
leadframe	Nickel	7440-02-0	C150001	0.257318	0.7350	2.0900	alloy,inner plating
leadframe	Copper	7440-50-8	C160001	12.028237	34.4000	97.6000	alloy,plating
leadframe	Tin	7440-31-5	C260001	0.012064	0.0345	0.0979	alloy,lead finish
leadframe	Palladium	7440-05-3	C310006	0.021360	0.0610	0.1730	inner plating
leadframe	Gold	7440-57-5	C310010	0.003390	0.0097	0.0275	inner plating
			sub_total	12.322369	35.2000	100.0000	
die bonding	Silver	7440-22-4	C170001	0.072360	0.2070	80.4000	electric conductor
die bonding	Epoxy resin	none	C670001	0.017640	0.0504	19.6000	adhesive
			sub_total	0.090000	0.2570	100.0000	
wires	Gold	7440-57-5	C310010	0.029089	0.0831	100.0000	wiring
			sub_total	0.029089	0.0831	100.0000	
encapsulation	Fused quartz	60676-86-0	C020013	14.429712	41.2000	78.1000	chief element
encapsulation	Other organic phosphorus compounds	298-00-0 etc.	C339999	0.048960	0.1400	0.2650	hardening
encapsulation	Epoxy resin	none	C670001	3.988800	11.4000	21.6000	base resin
			sub_total	18.467472	52.8000	100.0000	
			grand_total	35.000000	100.0000	0.0000	eQ019980.dbf SQ019980.DBF

PART : components, RENE_CODE : Our control no., MASS_MG : mass (mg)
RATIO : wt% on the total mass, RATIO_P : wt% on each site's mass
ppm on the total mass = RATIO x 10000 ppm on each part's mass= RATIO_P x 10000

*This data is called IMDS(International Material Data System) data calculated from designed data.
It shows 100 percent content of intentionally contained substances.

Sincerely Yours,
Renesas Technology Corporation

Makoto Tanaka
Manager
Corporate Environment and Safety Strategic Planning Dept.

RENESAS

To: Apple Inc.

Renesas Technology Statement Regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH)

This document is Renesas Technology's statement regarding Regulation (EC) No 1907/2006 of European Parliament and of the Council of 1 June 2007 concerning the Registration, Evaluation, Authorization, and of Restriction of Chemicals (REACH).

Renesas part (product) number;
R5H30201NA04NQ01GZ, R5H30201NA04NQ03GZ
R5H30201NA04NQ07GZ, R5H30201NA04NQ08GZ,
R5H30201NA04NQ09GZ, R5H30201DA04SP03

We hereby declare that products manufactured by Renesas Technology do not contain substances on the REACH SVHC candidate list in the table below.

Table 1. Candidate List of Substances of Very High Concern (SVHC)

No	Substance name	CAS number	EC number
1	Anthracene	120-12-7	204-371-1
2	4,4'-Diaminodiphenylmethane	101-77-9	202-974-4
3	Dibutyl phthalate	84-74-2	201-557-4
4	Cobalt dichloride	7646-79-9	231-589-4
5	Diarsenic pentaoxide	1303-28-2	215-116-9
6	Diarsenic trioxide	1327-53-3	215-481-4
7	Sodium dichromate	7789-12-0	234-190-3
8	5-tert-butyl-2,4,6-trinitro-m-xylene (musk xylene)	81-15-2	201-329-4
9	Bis(2-ethyl(hexyl)pthalate) (DEHP)	117-81-7	204-211-0
10	Hexabromocyclododecane (HBCDD) and all major diastereoisomers identified (α-HBCDD, β-HBCDD, γ-HBCDD)	25637-99-4	247-148-4
11	Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins)	85535-84-8	287-476-5
12	Bis(tributyltin)oxide	56-35-9	200-268-0
13	Lead hydrogen arsenate	7784-40-9	232-064-2
14	Benzyl butyl phthalate	85-68-7	201-622-7
15	Triethyl arsenate	15606-95-8	427-700-2

Renesas Technolory Corporation

Nobuyuki Ishii

Nobuyuki Ishii
Senior Engineer
Corporate Enviroment and Safety Strategic Planning Dept.
CSR Management Div.
Date: 16 April 2009

RENESAS

Report No. MAR-6001
Date : Oct. 3rd. 2008

To : Apple Inc.

RENESAS SEMICONDUCTOR
RELIABILITY REPORT

DEVICE : R5H30201NA04NQ Series

APPLICATION : Consumer

Reported by M. Ishiyama
M. Ishiyama

Confirmed by A. Nakanishi
A. Nakanishi

Approved by Y. Hosokawa
Y. Hosokawa

MCU Quality Assurance Dept.
Quality Assurance Div.
Renesas Technology Corp.

Caution

Notes :

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5. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
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(2) surgical implantations
(3) healthcare intervention (e.g., excision, administration of medication, etc.)
(4) any other purposes that pose a direct threat to human life
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8. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.

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1. INTRODUCTION

R5H30201NA04NQ Series are devices developed with Renesas 0.18um CMOS design rule, wafer process and Renesas standard package. This reliability report is the summary of the reliability test results at development and production of this device.

2. MAIN FEATURE

Product name	Type	Outline	Operating voltage	Use
16bit Smartcard MCU	R5H30201NA04NQ01	VQFN (PVQN0020KB-A)	Vcc=1.8～3.6V (1～10MHz)	Consumer
	R5H30201NA04NQ02			
	R5H30201NA04NQ03			
	R5H30201NA04NQ04			
	R5H30201NA04NQ05			
	R5H30201NA04NQ06			
	R5H30201NA04NQ07			
	R5H30201NA04NQ08			

3. FAILURE RATE

The failure rate is estimated as follows.

81 FIT

Where : ・Ta = 40C ・Ea = 0.8eV ・Confidence Level = 60%

4. TEST RESULT

Test Name		Pre	Test Condition	Test Result NG(ps)/Test(ps)	Addition
High Temperature Operating Life			Ta=100C, Vcc=3.6V, t=1000h	0/96	
High Temperature storage			Ta=150C, t=1000h	0/22	
Low Temperature storage			Ta=-55C, t=1000h	0/22	
Temperature Humidity storage		*1	Ta=85C, RH=85%, t=1000h	0/22	
Temperature Humidity Bias		*1	Ta=85C, RH=85%, Vcc=3.6V, t=1000h	0/22	
Pressure Cooker Test		*1	Ta=121C, RH=100%, t=100h	0/22	Reference
Temperature Cycle		*1	-55C～150C, 1000cycles	0/22	
Thermal Shock			0C～100C, 100cycles	0/22	
Electric-Static Discharge	HBM		R=1.5kΩ, C=100pF, +/-2000V, once	0/5	
	CDM		+/-1000V, once	0/5	
	MM		R=0Ω, C=200pF, +/-200V, once	0/5	Reference
Latch-up(Pulse Current Injection)			I= +/-150mA	0/5	
Solderability			245C, Rosin type flux, t=5s	0/22	
Drop			h=0.75m, Maple tree board, 3times	0/22	
Resistance to Soldering Heat		*2	Infrared Reflow Soldering 255C, 30s, 3times(MAX260C)	0/22	
		*2	Air Reflow Soldering 255C, 30s, 3times(MAX260C)	0/22	
		*2	Package dipping, 260C, t=10s, 3times	0/22	
			Leads dipping, 350C, t=3s	0/22	
Program/Erase Cycling			85C, 100k cycles	0/66	
Data Retention		*3	85C, t=1000h	0/22	
		*3	25C, t=1000h	0/22	
		*3	-20C, t=1000h	0/22	

*) All electrical tests before and after the reliability tests are based on the individual product specification.

*1 Pretreatment Condition : 85℃65%RH24h+Infrared Reflow Soldering 255C, 30s, 3times(MAX260C)

*2 Pretreatment Condition : 85℃65%RH24h

*3 Pretreatment Condition : Program/Erase Cycling 100k cycles at 85C